

Features

- 10 to 15 MHz clock
- Resolution 16 bits
- SNR 96 dB
- Linearity 14 bits
- On-chip Linear Phase Filtering
- 100 mW output power at max volume
- Drives 16 or 32 Ω headphone jack
- Minimal external filtering required
- Available in TSMC 90 nm Digital CMOS
- Easily ported to other technologies

Applications

- Portable audio players
- General Purpose Audio DAC

Description

The Kaben Wireless Silicon KR-DAC-02-TSMC90-01 is a general purpose stereo audio $\Delta\Sigma$ DAC. It consists of a Verilog digital block (DAC_Digital) that can be auto-placed and-routed and an analog hard macro (DAC_Analog).

Benefits

When integrating the KR-DAC-02-TSMC90-01 DAC into any system platform, our engineers provide an optimized design for system-level integration and verification, fabrication, and maximum re-use. We make your systems design predictable and efficient across many processes and application areas.

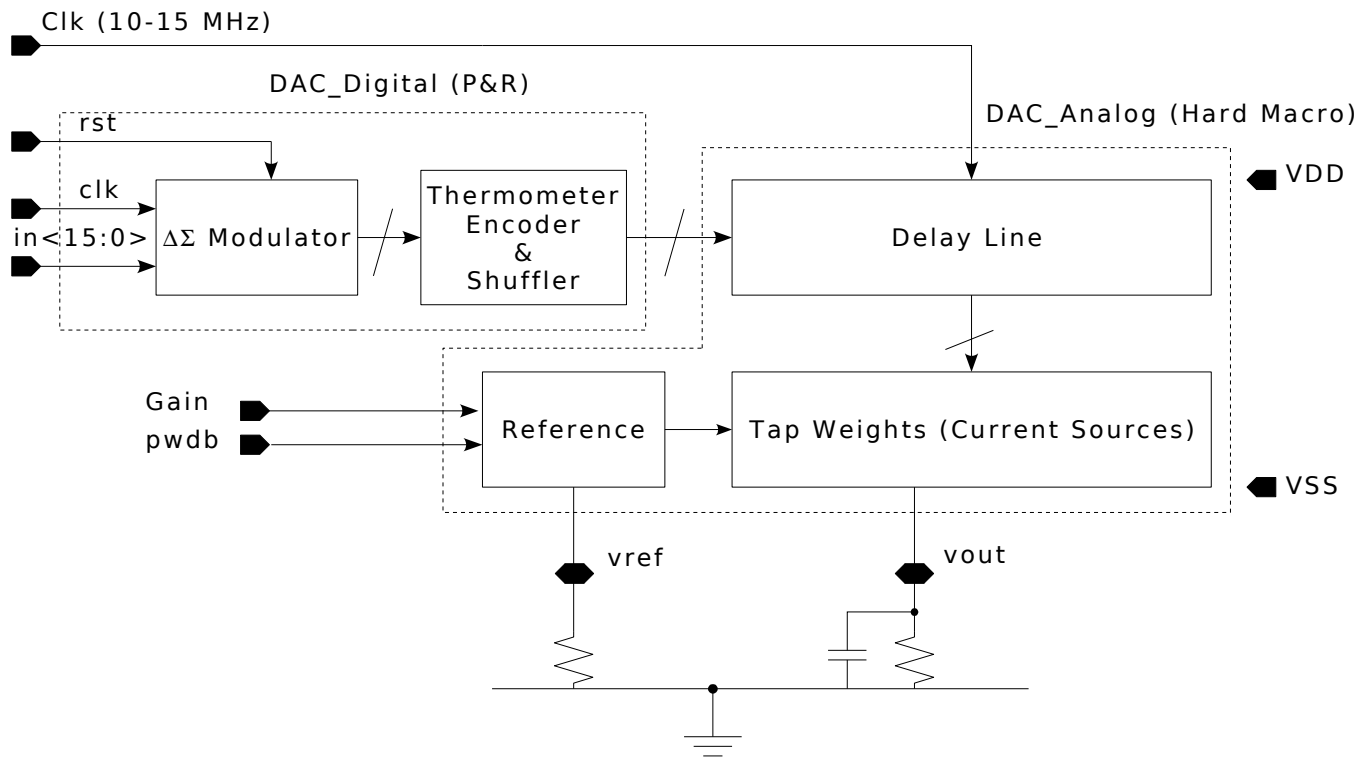
The design can be rapidly customized for audio applications in most CMOS foundry processes. Support includes tools for all phases of the life cycle of your SoC.

Kaben's $\Delta\Sigma$ stereo audio DAC can drive a headphone jack output directly and does not rely on component matching to achieve 14-bit linearity. As the linearity is achieved using delta-sigma techniques, the layout is more compact than traditional methods.

This architecture provides an interpolation filter after the $\Delta\Sigma$ DAC. This reduces the hardware complexity of the interpolation filter and eliminates the need for digital filtering before the $\Delta\Sigma$ DAC.

For system design, we provide a kit that includes high-level models in Matlab/Simulink, or Verilog/Verilog-A. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy.

At the circuit design level, we deliver GDS II files and a Cadence library containing schematics, symbols, and cell layouts. We also provide production test procedures for the cell.



KR-DAC-02-TSMC90-01 (one channel)

Electrical Characteristics

Parameter	Conditions	Min	Typical	Max	Units
Analog Supply Voltage		1.8	3.0	3.3	V
Analog Supply Current	10-15 MHz Clock, 32 Ω load			70	mA
	16 Ω load			95	mA
Digital Supply Voltage		1.0	1.1	1.2	V
Digital Supply Current				0.5	mA
Power Down Current				1	μ A
Resolution			16		Bits
Input Clock		10		15	MHz
Bandwidth				22	kHz
Channel Separation			30		dB
Output Power	16 or 32 Ω (Programmable)			100	mW
SNR	Single tone input full-scale, 22 kHz bandwidth		96		dB
SNDR	Under 2 tone Full-scale signal		84		dB
Operating Temperature		-40		+85	$^{\circ}$ C
Area	Analog		TBD		μ m
	Digital	Number of Inverter Equivalent Gates		TBD	Gates
		Placed and Routed with standard cells		TBD	