

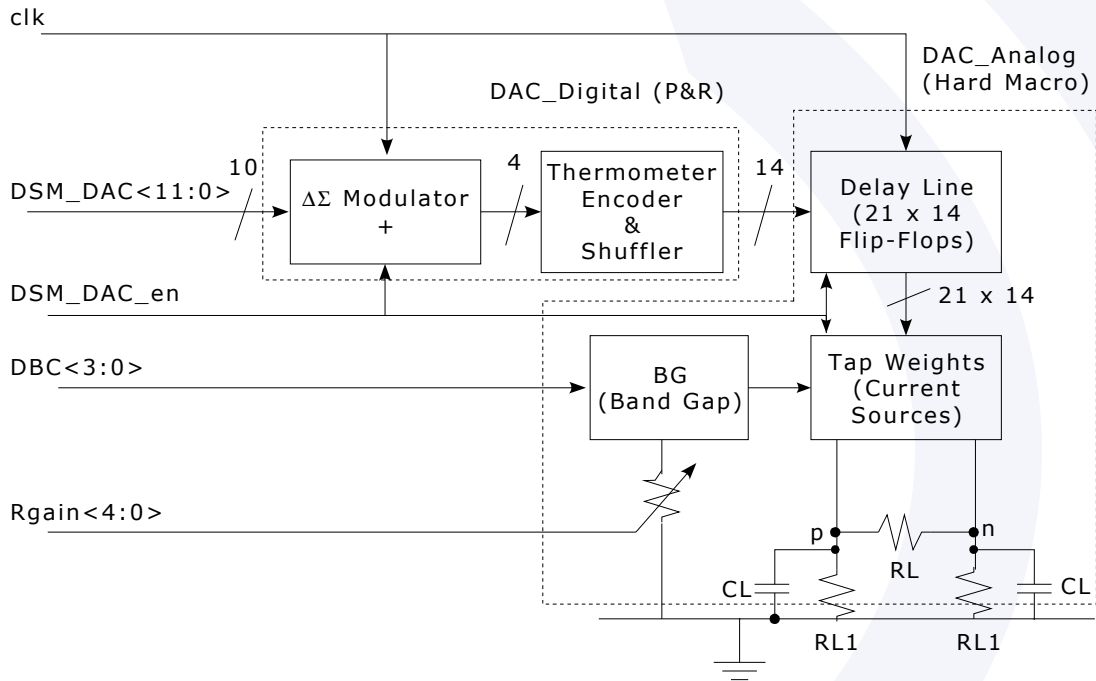
*"A 12-bit DAC IP Block  
Ready for Integrating into a Standard Product"*

**Features**

- Resolution 12 bits
- SNR 74 dB for 500 kHz Bandwidth
- INL and DNL +/-1 LSB
- Full-scale output current 1.14 mA to 10 mA programmable with 5 bits
- Current variation +/-5 % reducible to +/- 1% with external resistor
- Clock rate up to 40 MHz
- Turn on time 30  $\mu$ s
- Available in Jazz SiGe 60
- Portable to other BiCMOS technologies

**Applications**

- Wireless Transmitters
- General Purpose DAC



KR-DAC-40-JZ60-01

# 12 bit $\Delta\Sigma$ DAC

## KR-DAC-40-JZ60-01 Data Sheet

### Description

The Kaben Wireless Silicon KR-DAC-40-JZ60-01 is a general purpose 12 bit  $\Delta\Sigma$  DAC with a differential output. It consists of a Verilog digital block (DAC\_Digital) that can be auto-placed and-routed and an analog hard macro (DAC\_Analog).

When integrating the KR-DAC-40-JZ60-01 12 bit  $\Delta\Sigma$  DAC into any system platform, our engineers provide an optimized design for system-level integration and verification, fabrication, and maximum re-use. We make your systems design predictable and efficient across many processes and application areas.

The design can be rapidly customized for many BiCMOS foundry processes. Support includes tools for all phases of the life cycle of your SoC.

Kaben's 12 bit  $\Delta\Sigma$  DAC can drive up to 10 mA into a load. The full-scale output current is programmable from 1.14 mA to 10 mA using 5 bits making it very versatile for different applications. Output current

variation across process, supply and temperature is +/- 5 %. This can be reduced using an external resistor.

High linearity is achieved using delta-sigma techniques, making the layout more compact than competing solutions.

This architecture provides an interpolation filter after the  $\Delta\Sigma$  DAC. This reduces the hardware complexity of the interpolation filter and eliminates the need for digital filtering before the  $\Delta\Sigma$  DAC.

For system design, we provide a kit that includes high-level models in Matlab/Simulink, or Verilog/Verilog-A. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy.

At the circuit design level, we deliver GDS II files and a Cadence library containing schematics, symbols, and cell layouts. We also provide production test procedures for the cell.

### Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Analog Supply Voltage		2.7	3.0	3.6	V
Digital Supply Voltage		2.7	3.0	3.6	V
Analog Supply Current			48		mA
Digital Supply Current	Dependent on Customer Place and Route				mA
Power Down Current				4	$\mu$ A
Resolution			12		Bits
Input Clock		5	19.2	40	MHz
Bandwidth		133	510	1060	kHz
Full-Scale Output Current	Programmable with 5 bits. Current variation for any setting is 5 %.	1.14		10	mA
SNR	Single Tone Input Full Scale, 500 kHz bandwidth		74		dB
INL	Dynamic			+/- 1	LSB
DNL	Dynamic			+/- 1	LSB
THD	Full-Scale sinusoid		60		dB
Turn on time				30	$\mu$ s
Operating Temperature		-40		+85	$^{\circ}$ C
Area Analog			1,170,000		$\mu$ m <sup>2</sup>
Area Digital	Dependent on Customer Place and Route				$\mu$ m <sup>2</sup>

