

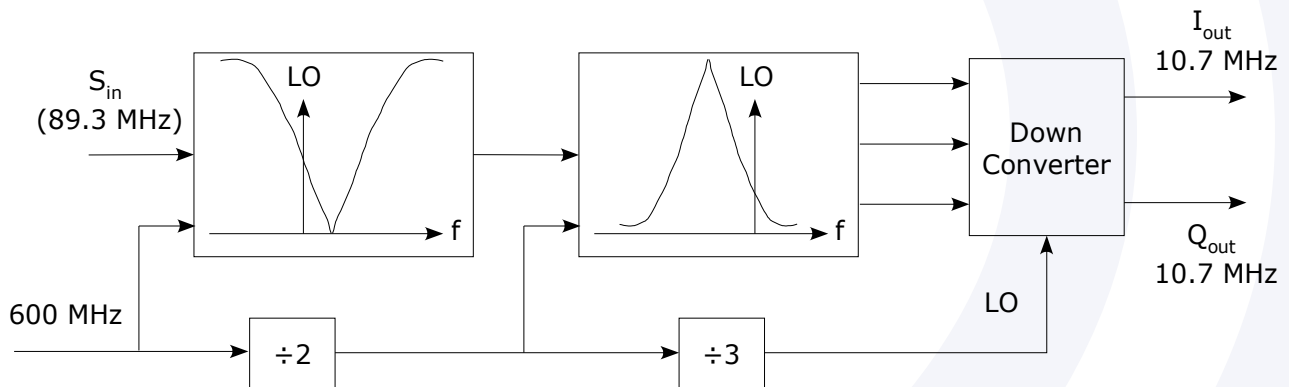
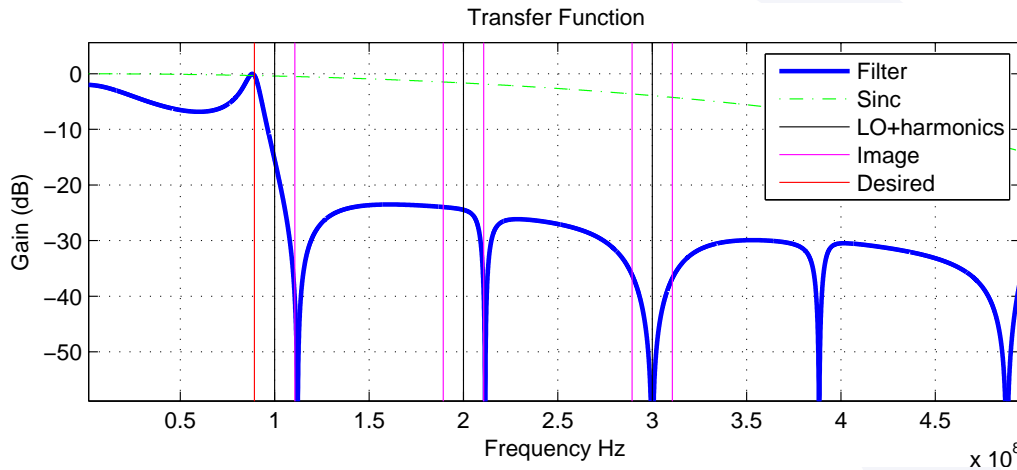
"The Industry's first on-chip Image Reject IF Filter/Down Converter for Integration into Multi-Standard Radios"

Features

- Programmable input frequency from 65 to 108 MHz
- 3 MHz Bandwidth at 89 MHz center frequency
- Output Frequency 10.7 MHz
- Image Frequency Notch Attenuation up to 40 dB
- Programmable Gain 20 dB in 2 dB steps
- Spurious Free Dynamic Range 90 dB
- Noise Figure 4 dB
- Low in-band Group Delay Distortion
- 3.0 V Operation
- Current Consumption 20 mA at 3 V
- Reduces ADC Sample Rates and Resolution
- Originally Designed for TSMC 130 nm process and portable to other processes

Applications

- FM Radios
- Bluetooth
- GPS
- Software Defined Radios (SDR)
- Multi-Standard Radios
- 2.4 and 5 GHz Radios



KR-SIF-IR-108-TSMC-130-01 Programmable Sampled-IF Filter

Image Reject Sampled-IF Filter/Down-Converter

KR-SIF-IR-108-TSMC-130-01 Preliminary Data Sheet

Description

Kaben's on-chip, image-reject filter/down-converter provides bandpass filtering of an input signal centered at 89.3 MHz, and down-conversion to an output center frequency of 10.7 MHz, with an image-rejection attenuation in excess of 30 dB. The image-reject filter is based on Kaben's patented Sampling IF (SIF) technology, which enables digital FIR and IIR filter techniques to be realized in RF. Since the bandpass center frequency and the image-reject notch frequency are controlled by the clock frequency, the on-chip filter response can be tuned to compensate for temperature variation and process corners.

The KR-SIF-IR-108-TSMC-130-01 filter consists of two cascaded SIF filters, the first establishing the notch frequency for image-rejection, and the second creating the bandpass response around the incoming signal. In order to take advantage of desirable impedance values obtainable in multi-conductor transmission lines, the sampled-analog output from the SIF filters is realized as a three-phase output. The filtered, three-phase, sampled-analog signal is then down-converted, translated into traditional in-phase and quadrature components, and reconverted to full analog format at 10.7 MHz.

The Kaben image-reject filter/down-converter significantly reduces the performance required by the associated ADC in any receiver. Since the additional dynamic range and bandwidth required to digitize potential adjacent channel blockers (in addition to the desired signal) is no longer required, the ADC becomes smaller, the sampling clock-rate becomes lower, the overall timing precision and digitizing linearity are relaxed, and the power consumption is reduced.

Support

For system's design, we provide a kit that includes high-level models in Matlab/Simulink, Systemview, and Verilog-A. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy.

At the circuit design level, we deliver GDS II files and a Cadence library containing schematics, symbols, and cell layouts.

Originally designed in the TSMC 130 nm process, this IP block can be ported to other technologies.

Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Input Frequency		65		108	MHz
Output Frequency			10.7		MHz
Loaded Q		29	30	31	
Spurious Free Dynamic Range	10 MHz Bandwidth	86	90		dB
Noise Figure			4	5	dB
Gain	2 dB steps	11		31	dB
Supply Current	Vcc = 3 V			20	mA
Supply Voltage		2.7	3.0	3.6	V
Operating Temperature		-40		85	°C

