

# A 4 GHz FRACTIONAL-N SYNTHESIZER FOR MULTI-MODE WIRELESS APPLICATIONS

**F**requency synthesizers are fundamental building blocks in any wireless system. The need for reducing component count in wireless systems continues to drive synthesizer integration onto single systems-on-a-chip (SoC). Many multi-standard wireless products are emerging with combinations of WLAN 802.11a/b/g, GSM, Bluetooth, GPS and CDMA.

One of the most challenging RF components to integrate on-chip is a high quality frequency synthesizer. Developing these multi-standard systems further increases the complexity, flexibility and performance requirements of the synthesizer. Wireless standards are usually planned around specific crystal frequencies. When a multi-standard design uses a crystal frequency from one standard it becomes a challenge to achieve the channel spacing required for any other standard. A single crystal frequency requires smaller step sizes in the synthesizer resulting in higher system phase noise. Kaben Research has addressed this need by introducing a  $\Delta\Sigma$  fractional-N frequency synthesizer intellectual property (IP) cell with very low phase noise and very fine step size.

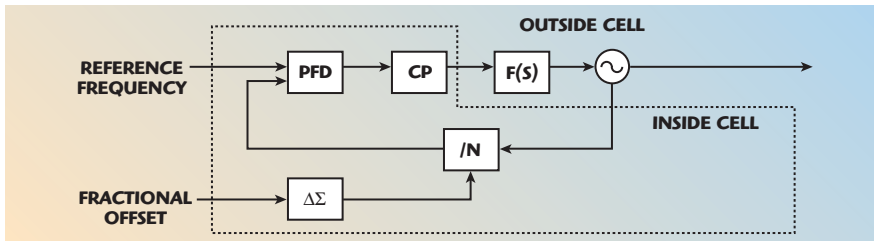
### BACKGROUND

There are two popular design trends in the wireless industry. The first is the integration of both RF and digital subsystems to create wireless SoCs. The second is integrating two or more wireless standards into the same chip. These two design trends raise the value proposition of a chip by increasing the functionality while shrinking cost and size. In the past simply delivering a working RF or digital chip would have been enough.

The demands on a wireless designer are increasing as the circuits become more complicated. Companies with leading edge IP in either RF or digital design are finding it increasingly difficult to attract the talent for designing all of the circuit components in wireless SoCs.

In the RF portion of any SoC, one of the most challenging circuits to design is a high quality frequency synthesizer able to deliver the desired frequency with a low phase noise. When that SoC integrates multiple wireless

# PRODUCT FEATURE



▲ Fig. 1 Block diagram of the KR-SDS45-ST6G  $\Delta\Sigma$  fractional-N frequency synthesizer.

standards, the demands on the synthesizer's performance increase because it must meet the most stringent requirement of any one of these multiple standards.

Multi-standard SoCs have a separate problem because different standards rarely use the same crystal frequency. A natural system design goal would be to use a single crystal. As an example, two widely used systems will be chosen: a GSM system using a 13 MHz crystal and a GPS system using a 10.23 MHz crystal. In a GSM system, the synthesizer divides the 13 MHz crystal frequency by 65, making all the channels an integer multiple of 200 kHz.

If a GSM system uses the GPS crystal, then achieving the 200 kHz system step size using an integer-N frequency synthesizer would be difficult because the division ratio ( $N$ ) of 10.23 MHz/200 kHz or 51.15 is not an integer. The crystal frequency would need to be divided by a much larger  $N$  to find a suitable frequency that can then be multiplied up to the 200 kHz step size. In this case the system phase noise suffers because of a larger  $20\log(N)$  phase noise contribution from the synthesizer. Another alternative is to use several synthesizers taking up additional real estate on the chip and consuming more power. This would seem to be the opposite direction for increased integration.

A more elegant approach to this problem is to integrate a fractional-N frequency synthesizer that has a very fine resolution. The synthesizer resolution would need to achieve the system step size using any crystal frequency while maintaining a low synthesizer phase noise.

The proposed solution is a  $\Delta\Sigma$  fractional-N frequency synthesizer because this type offers a very fine resolution without incurring the penalty of increased phase noise. In a  $\Delta\Sigma$  synthesizer, the step size is related to the crystal frequency and the num-

ber of bits in the  $\Delta\Sigma$  modulator.

Consider a fractional-N synthesizer with a 20-bit  $\Delta\Sigma$  modulator applied to the previous example. If the GPS crystal frequency is used, the step size would be 10.23 MHz/ $2^{20}$  giving roughly 9.76 Hz. This translates to less than  $\pm 5$  Hz frequency error. This level of error at the RF output is typically smaller than the frequency error caused by the crystal. Using the GSM crystal yields 13 MHz/ $2^{20}$  or approximately 12.4 Hz or  $\pm 6.2$  Hz error. If a finer resolution were required to achieve a smaller frequency error, then the number of bits in the  $\Delta\Sigma$  modulator could be increased. The result is that any output frequency can be derived from any crystal frequency when using a  $\Delta\Sigma$  frequency synthesizer.

The  $20\log(N)$  phase noise contribution from a  $\Delta\Sigma$  frequency synthesizer is much smaller than the integer-N method. In a  $\Delta\Sigma$  synthesizer,  $N$  is calculated by dividing the output frequency of the synthesizer by the crystal frequency, whereas in the integer-N synthesizer,  $N$  is the output frequency divided by the step size. In a  $\Delta\Sigma$  synthesizer the value of  $N$  remains the same regardless of the number of bits in the  $\Delta\Sigma$  modulator, meaning that the phase noise is unrelated to the channel step size.

In the case of the GSM system, the difference in the value of  $N$  between an integer-N and  $\Delta\Sigma$  fractional-N synthesizer is 13 MHz/200 kHz or 65 (there is an additional contribution of  $N$  based on the crystal frequency multiplied up to the synthesizer output frequency; however, both approaches have the same additional contribution). Now  $20\log(65)$  is roughly 36 dB. To make the comparison complete there is a  $10\log(N)$  phase noise benefit when dividing down the crystal frequency. Thus, in this case,  $10\log(13 \text{ MHz}/200 \text{ kHz})$  or  $10\log(65)$  is roughly 18 dB. This leaves an overall benefit to the  $\Delta\Sigma$

modulator synthesizer of 36 dB–18 dB = 18 dB.

If an integer-N synthesizer is used in a GSM system using a crystal frequency from another standard, the crystal frequency must be divided down to a fraction of the step size and then multiplied back up to an integer multiple of the step size. This increases the synthesizer phase noise contribution making the task of meeting the system specifications extremely difficult. Also, the  $10\log(N)$  benefit, when dividing down the crystal frequency, is limited to reaching the synthesizer noise floor. However, the  $20\log(N)$  contribution when multiplying back up continues to grow. The  $\Delta\Sigma$  fractional-N synthesizer does not have the same limitation when using different crystal frequencies and is therefore a superior solution.

Since a suitable solution for a frequency synthesizer in a multi-standard wireless SoC is a  $\Delta\Sigma$  fractional-N frequency synthesizer, the problem shifts to the task of designing one. SoC companies are already struggling to build up the design teams for the RF and digital systems. Designing a high quality on-chip integer-N synthesizer has always been recognized as a difficult task; a  $\Delta\Sigma$  fractional-N synthesizer is a specialized task with only a handful of experts available. Developing the in-house design expertise to build a few of these synthesizers is difficult, costly and time consuming. For many startups and fabless semiconductor companies this does not make economical sense.

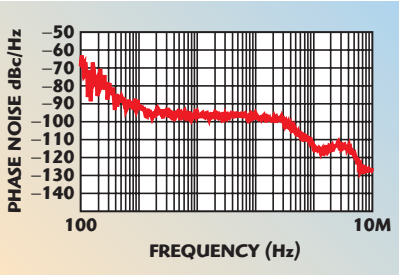
An alternative to designing specialized components is to license existing cells from IP vendors. The licensing model reduces costs, associated risk factor and design time when compared to developing specialized components in-house.

## FRACTIONAL-N FREQUENCY SYNTHESIZER CELL

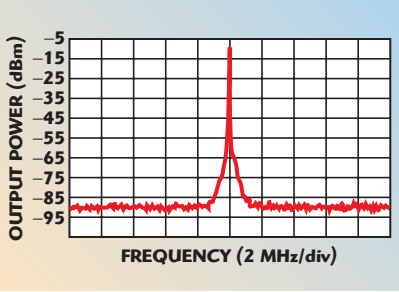
Kaben Research has designed and tested a 4 GHz  $\Delta\Sigma$  fractional-N frequency synthesizer cell with 20 bits of resolution. The KR-SDS45-ST6G can be licensed for quick integration into any design fabricated in the STMicroelectronics BiCMOS6G process. The cell will also be ported to several popular CMOS and BiCMOS processes.

Although the synthesizer IP was designed to be integrated into an

# PRODUCT FEATURE



▲ Fig. 2 Phase noise measurement at 2.434 GHz with a 300 kHz loop bandwidth.



▲ Fig. 3 Spurious response measurement at 2.434 GHz with a 50 kHz loop bandwidth.

SoC, the cell was fabricated and packaged as a standalone chip in order to verify and measure its performance. **Figure 1** shows the block diagram for a  $\Delta\Sigma$  fractional-N frequency synthesizer. The phase/frequency detector, charge pump, 20-bit  $\Delta\Sigma$  modulator, VCO divider and crystal oscillator have been integrated into a

single cell in STMicroelectronics 0.35  $\mu\text{m}$  BiCMOS6G technology. The loop filter and VCO are off chip.

## MEASURED RESULTS

The KR-SDS45-ST6G synthesizer measurements were performed on a standalone chip mounted on a custom socket on a FR4 printed circuit board. The board was powered by a 2.7 to 3.6 VDC supply. The measurements were made using a spectrum analyzer with a phase noise analysis module. A 16 MHz crystal was used with the on-chip oscillator. The output frequency was 2.43 GHz. A 300 kHz loop bandwidth was used for the phase noise measurements to suppress the VCO noise to clearly view the synthesizer phase noise contribution. Other performance measurements are listed in **Appendix A**.

The phase noise measurement in **Figure 2** shows a  $-96$  dBc/Hz synthesizer noise floor inside the loop bandwidth. The  $1/f$  noise is not visible above 2 kHz away from the carrier. The quantization noise generated by the  $\Delta\Sigma$  modulator is visible between 1 and 7 MHz away from the carrier. This quantization noise is easily suppressed by reducing the loop bandwidth or by using a higher frequency crystal. The spectrum analyzer plot in **Figure 3** shows no spurious tones above the noise floor.

## CONCLUSION

$\Delta\Sigma$  fractional-N synthesizers are a superior solution for integrating into multi-standard SoCs because the fine frequency resolution and low phase noise allows for a single crystal reference frequency. The demonstrated performance of the KR-SDS45-ST6G matches any commercially available synthesizer chip and is available for integration into user's SoCs thereby eliminating the need to build a highly specialized team to develop the component in-house. For additional information, contact Seste Dell'Aera at [seste.dellaera@kabenresearch.com](mailto:seste.dellaera@kabenresearch.com).

## References

1. Perrott, et al., "A 27 mW CMOS Fractional-N Synthesizer Using Digital Compensation for 2.5 Mb/s GFSK Modulation," *IEEE Journal Solid-State Circuits*, Vol. 32, No. 12, December 1997, pp. 2048–2060.
2. T.A.D. Riley and M.A. Copeland, "A Simplified Continuous Phase Modulator Technique," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 41, No. 5, May 1994, pp. 321–328.
3. N.J.R. King, "Phase Locked Loop Variable Frequency Synthesizer," US Patent 4,204,174.
4. N. Wells, "Frequency Synthesizer," US Patent 4,609,881.

**Kaben Research,**  
**Ottawa, Ontario, Canada**  
**(819) 684-3379,**  
**[www.kabenresearch.com](http://www.kabenresearch.com)**

## APPENDIX A

### MEASURED PERFORMANCE OF THE KR-SDS45-ST6G FRACTIONAL-N SYNTHESIZER

Parameter	Conditions	Minimum	Typical	Maximum
Supply voltage (VDC)		2.7		3.6
Supply current (mA)			6.3	
RF input operating frequency (MHz)		384		4000
Synthesizer contribution to close-in phase noise (dBc/Hz)	16 MHz crystal 2.43 GHz RF signal 2 kHz offset		-95	
Spurious response (dBc)	Spurious within the loop bandwidth close to integer multiple of the reference frequency			-50
	Spurious greater than four loop bandwidths away from integer multiple of the reference frequency		-80	-74
	Spurious at integer multiple of the reference frequency		-80	-74
Operating temperature ( $^{\circ}\text{C}$ )		-40		+85