

General Description

The KWS120-XL-OSC is a high performance, low noise, low-power crystal oscillator IP block designed to operate with a 40 MHz AT Cut Fundamental mode crystal. Only 2 external capacitors are required to support startup operation and deliver desired frequency accuracy. Low power delivery supports sleep mode operation.

Features

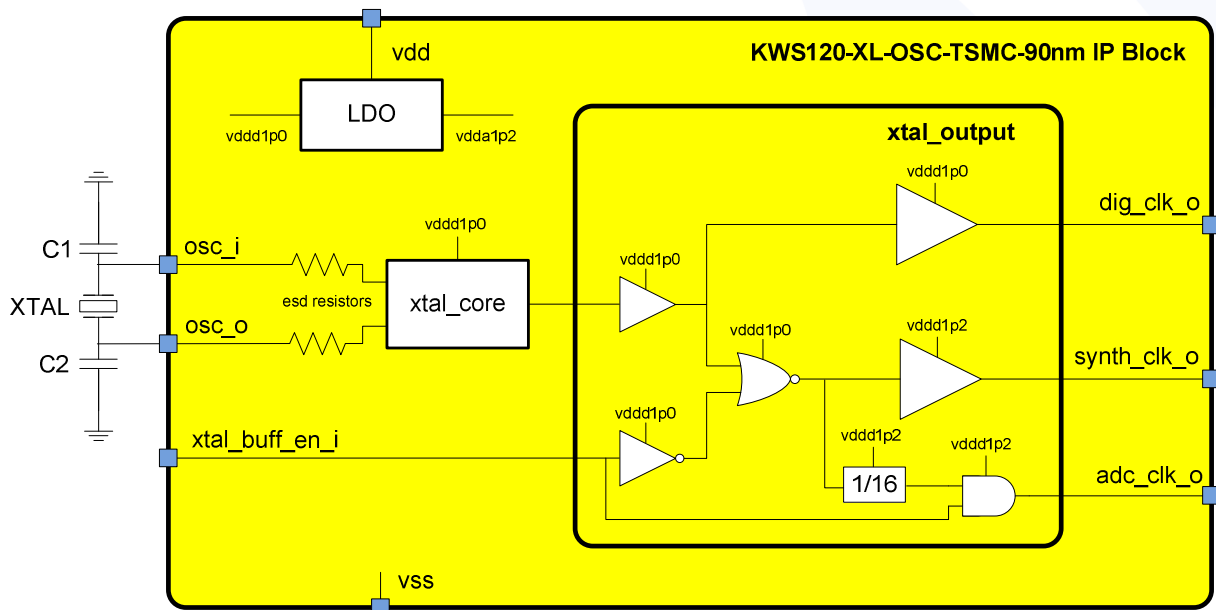
- Clock or Crystal Reference Frequency 40 MHz
- Low Phase Noise Contribution
- Supply Range 2.7-3.6 Volts
- Low Current Consumption 600 uA
- Area 0.06 mm²
- Operating Junction Temperature -20 to 110 °C
- Integrated 1.0/1.2 Volt Regulators
- Designed in TSMC 90 nm Process
- Wirebond and Flip Chip versions available

Applications

- PLL Synthesizer Reference Frequency Source
- Low Frequency ADC Sampling Clock
- Low Frequency Digital Circuit Clock

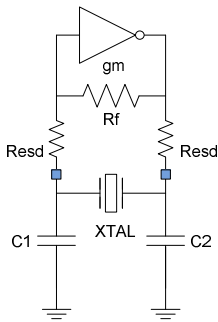
IP or Turnkey Solutions

- IP ready for integration into clients ASIC
- Standalone IC



Detailed Description

The KWS120-XL-OSC is based upon conventional Pierce-type crystal oscillator interface design that operates in the region of parallel resonance. The transconductance amplifier in the core provides 180 degrees of phase shift and the external capacitors provide the additional 180 degrees of phase shift to support sustained oscillation. The external crystal combined with capacitors C1 and C2 provides a frequency selective feedback path that tends to stabilize the frequency of operation. Feedback resistor Rf develops a bias for the transconductance amplifier that places it in the high gain linear region of operation. The transconductance amplifier is designed to ensure there is a suitable positive closed loop gain to promote start-up and sustain oscillation.



Deliverables

Kaben's Release Kit contains GDSII files and encrypted netlists, Verilog/Verilog-A files and a Conformance Report.

Support

When integrating the crystal oscillator cell into your design, our engineers support your effort from system-level integration through verification and fabrication. This characterized cell enables your SoC with predictable performance across multiple applications. Support is provided for all phases of the life cycle of your SoC. For system design Kaben provides high-level models in Matlab. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy. All high-level models are based on measured data. Customization of the design based upon a different set of crystal motional parameters is possible.

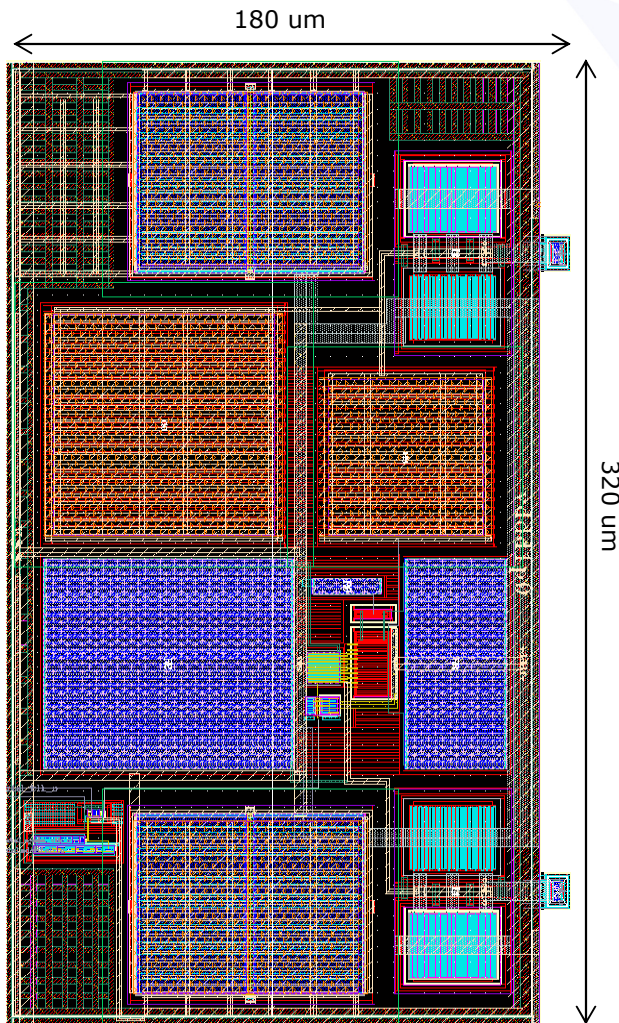
Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		2.7		3.6	V
Total Supply Current				600	uA
Integrated Regulator	+/-5%	0.95/1.14	1.0/1.2	1.05/1.26	V
Fundamental Mode Crystal Frequency			40		MHz
Start-Up Time			1.5		ms
External Capacitance	COG Type		20		pF
Transconductance		4.81	3.72	2.92	mA/V
Phase Noise	Offset = 10 Hz			-88	dBc/Hz
	Offset = 20 kHz			-146	
	Offset = 20 MHz			-162	
Operating Junction Temperature		-20	27	110	°C
Area	TSMC 90nm		0.06		mm ²

Pinout Description

Pin Name	IO	Function	Description
xtal-clk-o	O	Signal	40MHz 1V CMOS clock to digital
xtal-synth-clk-o	O	Signal	40MHz 1V CMOS clock to synth
xtal-adc-1f-clk-o	O	Signal	40MHz 1V CMOS clock to ADC
xtal-buff-en-i	I	Signal	Active high Buffer Enable
osc-i	I	Signal	Input from external crystal
osc-o	O	Signal	Feedback to external crystal
vdd	IO	Power	Power supply to internal regulator
vss	IO	Power	Ground return for crystal cell

Layout



RC Extracted Simulation Results

