

General Description

The KWS401 is a low-noise, Integer-N multiplying Delay-Locked Loop (DLL) that synthesizes a default 144MHz frequency from a 16MHz reference clock, or alternatively from a XL (when used in conjunction with the KWS110 XL Oscillator). The frequency range may be extended as an option so the output of the DLL may synthesize a range of frequencies between 100-400MHz. This DLL may optionally be configured as a multiphase clock generator as well.

Features

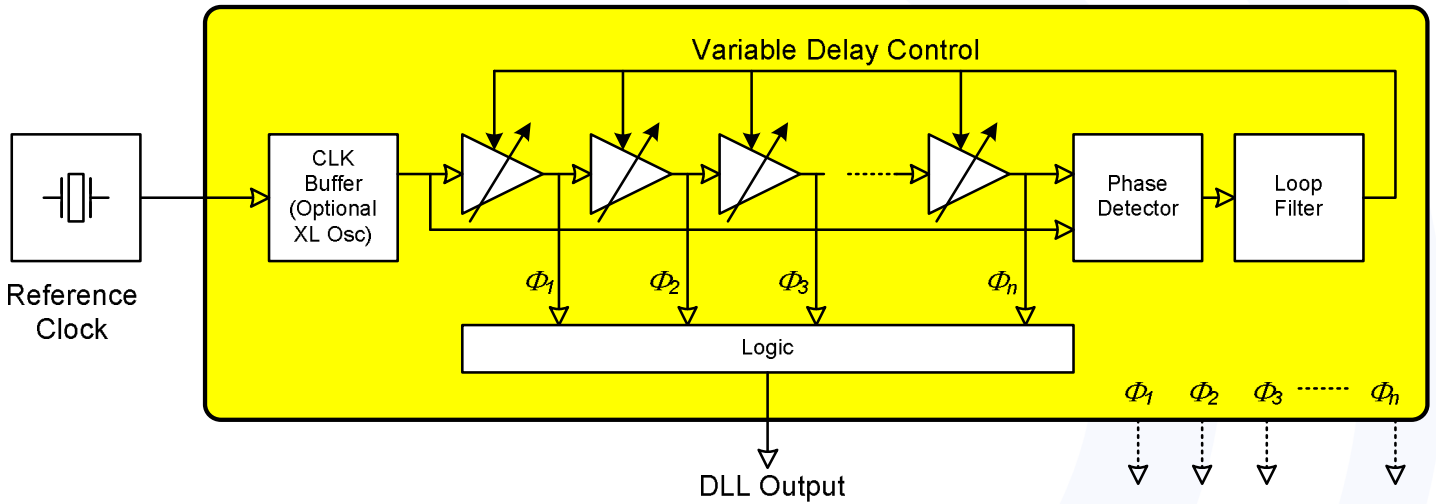
- Input Clock Frequency 16MHz, optional 10-20MHz
- Number of Delays Stages 9, optional 3 to 20
- Output Frequency 144MHz, optional 100-400MHz
- RMS Timing Jitter < 3ps RMS
- Supply 2.7-3.6V, internally regulated
- Current Consumption 4mA
- Integrated Regulator 1.2V
- Designed in TSMC 130nm process
- Area 0.26mm²

Applications

- Clock and Data Recovery
- SerDes
- Multiple Phase Clock Generation
- Digital ASICs/Microprocessors
- Clock Skew Correction
- Secondary LO / CLK

Turnkey Solutions

- IP ready for integration into clients ASIC
- Standalone IC may be made available
- Portable and option customization available



KWS401

Detailed Description

A Delay Lock Loop provides a small, low cost, lower power consumption alternative to a more complex phase locked, integer N frequency synthesizer. It can also be used to provide a selectable phase shift (time delay) of an input clock. These advantages result from the lack of a requirement for a Voltage Controlled Oscillator in the DLL. However, a DLL does present a significantly reduced choice of frequencies, and usually delivers a higher phase noise level and larger reference clock feed-through spurs.

Unlike other Delay Lock Loops, the Kaben KWS401 144MHz Integer-N Delay-Locked Loop provides a low phase noise output at an integer multiple of an input clock. The low phase noise is achieved through a combination of judicious transistor size selection and layout, power regulator design, and a DLL loop architecture which minimizes noise accumulation (as would occur if the delay stages of the DLL were arranged simply as a ring oscillator). The Kaben DLL is available in a range of standard CMOS processes, and does not require any special process features (such as thick metal for inductors, or deep N wells

for isolation).

The variable delay elements of the DLL consist of current controlled, inverter cells, charging interstitial capacitors. The output of a string of the delay cells is compared in phase with the input reference clock to produce the error signal. This error signal regulates the current controls for the delay cells, thus forming a first order feedback loop.

Depending on the logic configuration and on the value of N (the number of delay elements) utilized, the frequency of the output signal can be selected as any integer factor of N, where N is the number of variable delay elements utilized. It should be noted that, depending on the number of delay elements utilized and the integer factor selected, the duty cycle may vary from a 50 % value.

Support can be provided for all phases of the life cycle of your chip. For system design, we provide a kit that includes high-level models in Matlab/Simulink. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy.

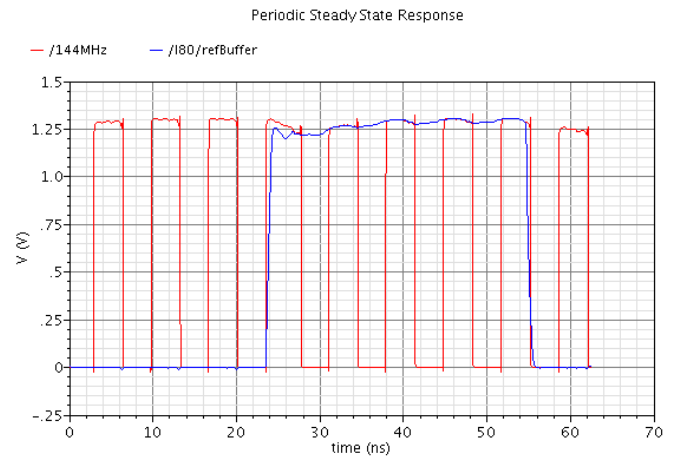
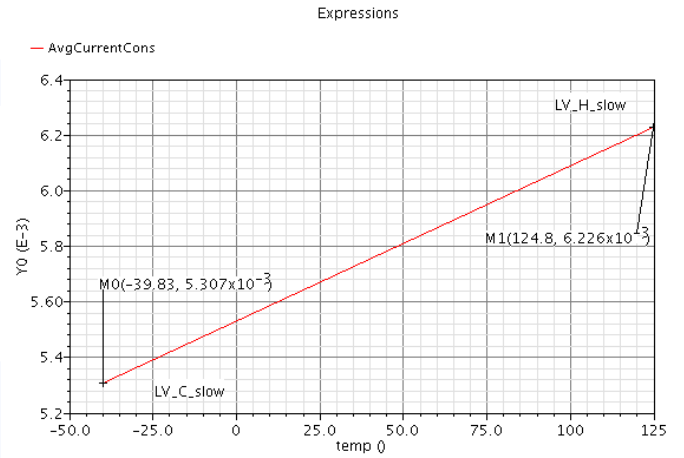
Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		2.7	3.3	3.6	V
Integrated Regulator			1.2		V
Total Supply Current			6		mA
Input Clock Frequency		10	16	20	MHz
Number of Delay Stages		3	9	20	
Output Frequency		100	144	400	MHz
Phase Noise	Offset = 100 Hz		-104		dBc/Hz
	Offset = 1 kHz		-114		
	Offset = 10 kHz		-116		
	Offset = 100 kHz		-119		
Reference Feedthrough Spur Levels				-30	dBc
Operating Temperature		-40	27	100	°C
Area	in TSMC 130nm		0.26		mm ²

Pinout Description

IO Name	IO	Function	Description
refin	I	Signal	Reference clock or output from XL cell
clk-144-mhz	O	Signal	144 MHz output clock
clk-144mhz-tst	O	Signal	144 MHz output clock to offship
pdb	I	Control	Power down control
por	I	Control	Post startup up power-on-reset
vc-init	I	Control	Initialize control voltage to low or high
vbias-prog[1:0]	I	Control	Two bits to control delay element speed
ibias-prog[1:0]	I	Control	Two bits to control charge pump current
vdd	IO	Power	Power supply to internal regulator
vss	IO	Power	Ground return for clock cell

RC Extracted Simulation Results



Layout

