

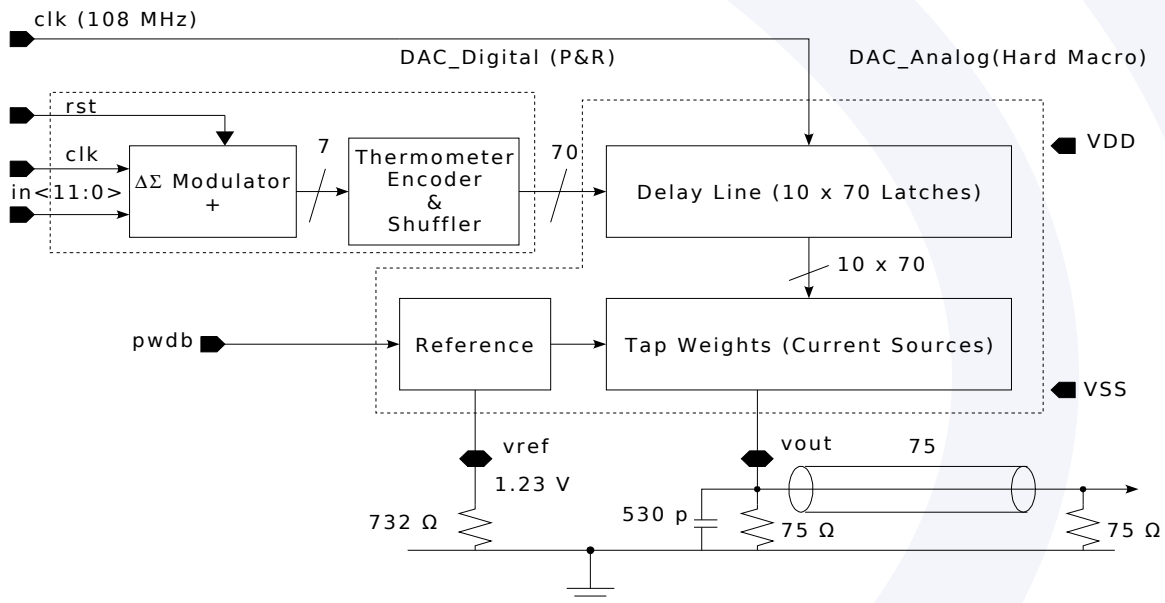
*"A Video DAC IP Block
Ready for Integrating into a Standard Product"*

Features

- Compact design
- Up to 108 MHz Clock
- Resolution 12 bits
- Bandwidth 8 MHz
- Output Current Range 20 to 35 mA
- Drives Double Terminated 75 Ω output
- Available in TSMC 0.13 μm CMOS
- Easily ported to other technologies

Applications

- Standard NTSC Video
- Standard PAL Video
- General Purpose D/A



KR-DAC-06-TSMC13-01

$\Delta\Sigma$ Baseband Video DAC

KR-DAC-06-TSMC13-01 Data Sheet

Description

The Kaben Wireless Silicon KR-DAC-06-TSMC13-01 is a general purpose $\Delta\Sigma$ Video Baseband D/A Converter that can drive a double terminated 75 Ω output for NTSC video applications. It consists of a Verilog digital block (DAC_Digital) that can be auto-placed and-routed and an analog hard macro (DAC_Analog).

When integrating the KR-DAC-06-TSMC13-01 D/A Converter into any system platform, our engineers provide an optimized design for system-level integration and verification, fabrication, and maximum re-use. We make your systems design predictable and efficient across many processes and application areas.

The design can be rapidly customized for NTSC video applications in most CMOS foundry processes. Support includes tools for all phases of the life cycle of your SoC.

Kaben's $\Delta\Sigma$ Video Baseband D/A Converter can drive a 75 Ω double terminated output and does not rely on component matching to achieve 10-bit linearity. As the linearity is achieved using delta-sigma techniques, the layout is more compact than competing solutions.

This architecture provides an interpolation filter after the $\Delta\Sigma$ D/A. This reduces the hardware complexity of the interpolation filter and eliminates the need for digital filtering before the $\Delta\Sigma$ D/A.

For system design, we provide a kit that includes high-level models in Matlab/Simulink, or Verilog/Verilog-A. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy.

At the circuit design level, we deliver GDS II files and a Cadence library containing schematics, symbols, and cell layouts. We also provide production test procedures for the cell.

Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Analog Supply Voltage		2.7	3.3	3.6	V
Analog Supply Current	108 MHz Clock. 35 mA output current.	29	37	42	mA
Digital Supply Voltage		1.08	1.2	1.32	V
Digital Supply Current				0.5	mA
Power Down Current				1	μ A
Resolution			12		Bits
Input Clock			108		MHz
Bandwidth				8	MHz
Full Scale Output Voltage	37.5 Ohm load. Programmable with external reference resistor.	0.7	1.0	1.3	V
Full Scale Output Current	37.5 ohm load. Programmable with external reference resistor. Current variation for any setting is 5 %.	20	27	35	mA
SNR	Single tone input full-scale, 8 MHz bandwidth	57			dB
SNDR	Under 2 tone Full-scale signal	56			dB
INL	Static			+/-1	LSB
Operating Temperature		-40		+85	$^{\circ}$ C
Area	Analog				
	Digital	Number of Inverter Equivalent Gates		11,296	Gates
		Placed and Routed with standard cells		181,000	μ m ²

