Fractional-N Synthesizer 0.6 – 3 GHz

KR-SDS-30-JZ60-01 Data Sheet

Features

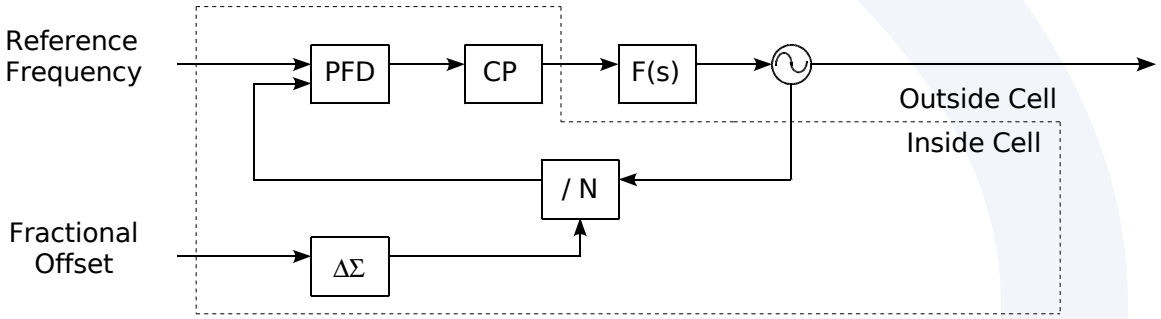
- Designed for Jazz SiGe 60 Process
- Fine step size of 60 Hz with 30 MHz reference frequency
- 20-bit ΔΣ Modulator
- Phase noise –105 dBc/Hz at 20 kHz offset at 3 GHz with 30 MHz reference
- Spurious response -80 dBc
- Reference frequency up to 30 MHz
- Simple integration into existing designs
- 600 MHz to 3 GHz operation
- 2.7 to 3.6 V operation
- Current consumption 8 mA at 3 V
- Digitally Filtered Lock Detect

Applications

- WLAN 802.11a, 802.11b, 802.11g
- Bluetooth
- GSM
- Multi-mode Radios
- Satellite Receivers
- 2-Way Pagers
- Cable Modems
- PCS/PCN
- 2-Way Radios
- CDMA Systems

Options

- Kaben can incorporate a proprietary integrated Loop Filter with performance matching off-chip loop filter designs



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Description

The Kaben KR-SDS-30-JZ60-01 Delta-Sigma (ΔΣ) Fractional-N frequency synthesizer cell provides fine step size, low phase-noise, low spurious levels, fast switching speed, and the ability to easily integrate into your current design. This synthesizer is a key building block in designing high-performance wireless systems that require fine resolution and low power.

When integrating the ΔΣ Fractional-N synthesizer core into your Jazz SiGe 60 SoC, our engineers support your design for system-level integration and verification, fabrication, and maximum re-use. This proven and characterized cell helps in making your SoC design predictable across many applications.

The Kaben KR-SDS-30-JZ60-01 cell has a maximum output frequency of 3 GHz while maintaining step sizes of 60 Hz using the 20-bit ΔΣ modulator making it ideal for multi-mode wireless systems.

The synthesizer cell uses a high internal reference frequency of up to 30 MHz to achieve a close-in phase noise of −105 dBc/Hz measured from a 3 GHz synthesizer.

Spurious response of −80 dBc makes this product an ideal selection for applications where interference from adjacent or alternate channels is a significant issue.

High performance is delivered without sacrificing power consumption. The cell operates using 8 mA from a 3 V supply.

Support can be provided for all phases of the life cycle of your SoC. For system design, we provide a kit that includes high-level models in Matlab/Simulink. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy. Included is a loop-filter design kit for tailoring the trade-off between VCO noise and synthesizer phase noise. All high-level models are based on measured data.

At the circuit design level, Kaben's Release Kit contains GDSII files, Verilog files, and Cadence™ design libraries containing test benches, schematics, symbols, and cell layouts.

For production test, the cell has a built-in Signature Analysis block.

Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		2.7	3.0	3.6	V
Total Supply Current	Vcc=3 V, Temp=25 °C, F_{REF}= 13 MHz, f_{VCO}=3 GHz not including digital		8		mA
RF Input Operating Frequency		0.6		3	GHz
Reference Oscillator Frequency		5	13	30	MHz
Charge Pump Output Current		.0625		4	mA
Current Step Size			62.5		µA
Charge Pump Variation Over Temperature				+/- 5	%
RF Input Sensitivity	Peak-to-peak single ended	150		300	mV
Synthesizer contribution to close-in Phase Noise	20 kHz offset at 3 GHz synthesizer output using a 30 MHz reference and charge pump current of 500 µA.		-98		dBc/Hz
	20 kHz offset at 3 GHz synthesizer output using a 30 MHz reference and charge pump current of 4 mA.		-105		
Spurious Levels	When carrier is within one Loop Bandwidth of an Integer multiple of the reference frequency			-60	dBc
	When carrier is more than 10 Loop Bandwidths away from an Integer multiple of the reference frequency		-80		
Integer Divider Range		100		30,000	
Frequency Resolution		$\frac{2 \cdot F_{REF}}{2^{20}}$			Hz
Operating Temperature		-40		+85	°C