

### Features

- Proven GDSII available for IBM 5HP
- Fine step sizes of 60 Hz with 32 MHz reference frequency using the programmable 20/10-bit  $\Delta\Sigma$  modulator
- Phase noise  $-95$  dBc/Hz at 10 kHz offset at 3.2 GHz with 19.2 MHz reference
- Spurious response  $-80$  dBc
- Internal Reference frequency up to 32 MHz
- Simple integration into existing designs
- 500 MHz to 3.2 GHz operation
- 2.7 V to 3.3 V operation
- Current consumption 11 mA at 3 V

### Applications

- WLAN 802.11a, 802.11b, 802.11g
- Bluetooth
- GSM
- Multi-mode Radios
- Satellite Receivers
- 2-Way Pagers
- Cable Modems
- PCS/PCN
- 2-Way Radios
- CDMA Systems
- Software Defined Radios

### Options

- Kaben can incorporate a proprietary integrated Loop Filter with performance matching off-chip loop filter designs

The Kaben KR-SDS-32-IBM5HP-01 Delta-Sigma ( $\Delta\Sigma$ ) Fractional-N frequency synthesizer cell provides fine step size, low phase-noise, low spurious levels, fast switching speed, and the ability to easily integrate into your current design. This synthesizer is a key building block in designing high-performance wireless systems that require fine resolution and low power.

When integrating the  $\Delta\Sigma$  Fractional-N synthesizer core into your IBM5HP SoC, our engineers support your design for system-level integration and verification, fabrication, and maximum re-use. This proven and characterized cell helps in making your SoC design predictable and efficient across many application areas.

The Kaben KR-SDS-32-IBM5HP-01 cell has a maximum output frequency of 3.2 GHz and its versatility makes it ideal for maximum reuse in a variety of wireless systems applications.

The synthesizer has a low close-in phase noise of  $-95$  dBc/Hz measured at a 3.2 GHz synthesizer output. Spurious response of  $-80$  dBc makes this product an ideal selection for narrowband applications that require very low spurs.

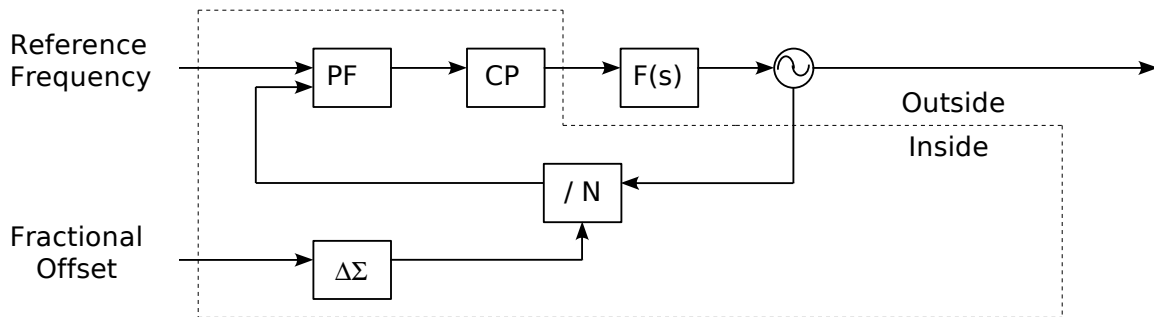
The cell uses a high internal reference frequency of up to 32 MHz for a very low phase noise contribution while maintaining step sizes of 60 Hz using the programmable 20-bit  $\Delta\Sigma$  modulator.

High performance is delivered without sacrificing power consumption. The cell operates using 11 mA from a 3 V supply.

Support can be provided for all phases of the life cycle of your SoC. For system design, we provide a kit that includes high-level models in Matlab/Simulink, Systemview, Verilog-A, and VHDL. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy. Included is a loop-filter design kit for tailoring the trade-off between VCO noise and synthesizer phase noise. All high-level models are based on measured data.

At the circuit design level, we deliver GDSII files and a Cadence library containing schematics, symbols, and cell layouts.

For production test, the cell has a built-in signature analysis block.



KR-SDS-32-IBM5HP-01

## Electrical Characteristics

Parameter	Conditions	Min	Typical	Max	Units
Supply Voltage		2.7		3.3	V
Total Supply Current	V <sub>CC</sub> = 3 V, Temp = 25°C F <sub>REF</sub> = 19.2 MHz F <sub>VCO</sub> = 3.2 GHz		11		mA
RF Input Operating Frequency		0.5		3.2	GHz
Reference Oscillator Frequency	Internal Reference Oscillator			32	MHz
Charge Pump Output Current	62.5 μA Step Size	62.5		1000	μA
Charge Pump Variation Over Temperature				+/- 5	%
RF Input Sensitivity	Peak-to-peak single ended	150		300	mV
Synthesizer contribution to close-in Phase Noise	F <sub>REF</sub> = 19.2 MHz RF signal = 3.2 GHz Offset = 10 kHz		-95		dBc/Hz
Frequency Resolution		$\frac{2 \cdot F_{REF}}{2^{20}}$			Hz
Spurious	When carrier is within one Loop Bandwidth of an Integer multiple of the reference frequency			-55	dBc
	When carrier is more than 10 Loop Bandwidths away from an Integer multiple of the reference frequency		-80	-75	
Operating Temperature		-40		+85	°C