

Features

- Proven GDSII available for STMicroelectronics BiCMOS6G
- Fine step sizes of 60 Hz with 32 MHz reference frequency using the programmable 20/10-bit $\Delta\Sigma$ modulator
- Phase noise -95 dBc/Hz at 2 kHz offset at 2.4 GHz with 16 MHz reference
- Spurious response -80 dBc
- Reference frequency up to 32 MHz
- Simple integration into existing designs
- Up to 4.5 GHz operation
- 2.7 to 3.6 V operation
- Low current consumption 5.3 mA at 3 V

Applications

- WLAN 802.11a, 802.11b, 802.11g
- Bluetooth
- GSM
- Multi-mode Radios
- Satellite Receivers
- 2-Way Pagers
- Cable Modems
- PCS/PCN
- 2-Way Radios
- CDMA Systems

Options

- Kaben can incorporate a proprietary integrated Loop Filter with performance matching off-chip loop filter designs
- Divide by 2 prescaler for VCO operation up to 6 GHz
- Minimum divide ratio of 12 from the VCO to the phase detector
- Digitally filtered lock detect
- 3-wire Serial Interface
- Internal Reference Oscillator
- Fast Acquisition improves lock 10 times faster for large frequency offset

The Kaben KR-SDS-45-ST6G-01 Delta-Sigma ($\Delta\Sigma$) Fractional-N frequency synthesizer cell provides fine step size, low phase-noise, low spurious levels, fast switching speed, and the ability to easily integrate into your current design. This synthesizer is a key building block in designing high-performance wireless systems that require fine resolution and low power.

When integrating the $\Delta\Sigma$ Fractional-N synthesizer core into your BiCMOS6G SoC, our engineers support your design for system-level integration and verification, fabrication, and maximum re-use. This proven and characterized cell helps in making your SoC design predictable and efficient across many application areas.

The Kaben KR-SDS-45-ST6G-01 cell has a maximum output frequency of 4.5 GHz and its versatility makes it ideal for maximum reuse in a variety of wireless systems applications.

The synthesizer has a low close-in phase noise of -95 dBc/Hz measured at a 2.4 GHz synthesizer output. Spurious response of -80 dBc makes this product an ideal selection for narrowband applications that require very low spurs.

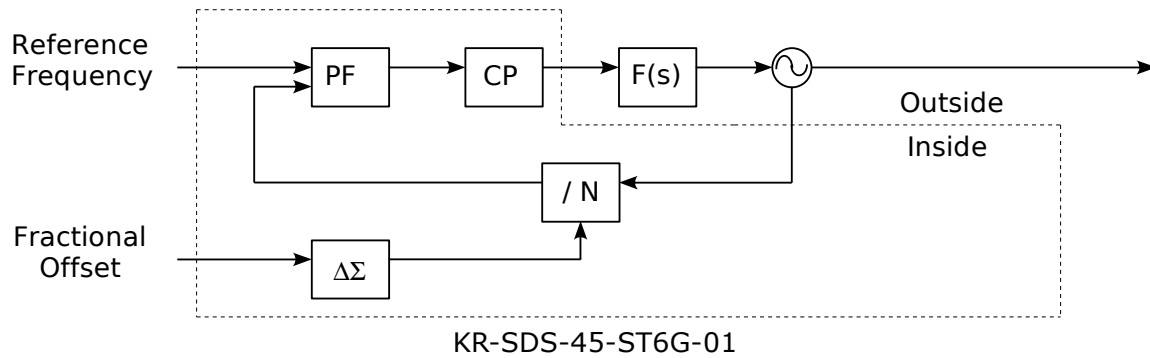
The cell uses a high internal reference frequency of up to 32 MHz for a very low phase noise contribution while maintaining step sizes of 60 Hz using the programmable 20-bit $\Delta\Sigma$ modulator.

High performance is delivered without sacrificing power consumption. The cell operates using 5.3 mA from a 3 V supply.

Support can be provided for all phases of the life cycle of your SoC. For system design, we provide a kit that includes high-level models in Matlab/Simulink, Systemview, Verilog-A, and VHDL. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy. Included is a loop-filter design kit for tailoring the trade-off between VCO noise and synthesizer phase noise. All high-level models are based on measured data.

At the circuit design level, we deliver GDSII files and a Cadence library containing schematics, symbols, and cell layouts.

For production test, the cell has a built-in signature analysis block.



Electrical Characteristics

Parameter	Conditions	Min	Typical	Max	Units
Supply Voltage		2.7		3.6	V
Total Supply Current	V _{CC} = 3 V, Temp = 22°C f _{REF} = 16 MHz DSM = 20-bit mode F _{IN} = 2.4 GHz		5.3		mA
RF Input Operating Frequency		400		4.5	GHz
Reference Oscillator Frequency	Internal Reference Oscillator			32	MHz
Charge Pump Output Current			500		μA
Charge Pump Variation Over Temperature				+/- 5	%
RF Input Sensitivity		150		300	mV
Synthesizer contribution to close-in Phase Noise	f _{REF} = 16 MHz RF signal = 2.4 GHz Offset = 2 kHz		-95		dBc/Hz
Spurious	Spurious within the Loop Bandwidth close to Integer multiple of the Reference Frequency			-50	dBc
	Spurious greater than four Loop Bandwidths away from Integer multiple of the Reference Frequency		-80	-74	
Operating Temperature		-40		+85	°C