

Features

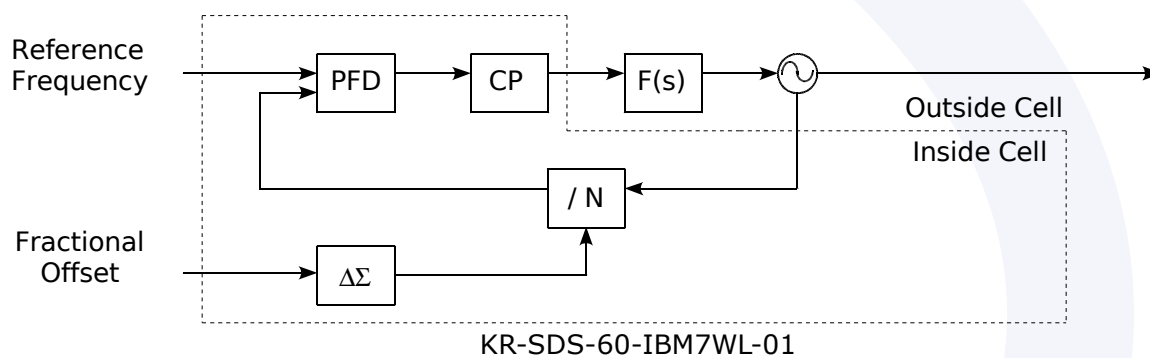
- 2 to 6 GHz operation
- Reference Frequency up to 40 MHz
- 20-bit $\Delta\Sigma$ Modulator gives step size of 40 Hz with 40 MHz reference frequency
- Phase noise -93 dBc/Hz at 2 kHz offset at 6 GHz with 20 MHz reference
- Spurious response -80 dBc
- Simple integration into existing designs
- 2.6 V to 3.0 V operation
- Current consumption 12.5 mA at 2.7 V
- Digitally Filtered Lock Detect
- Originally designed for IBM 7WL process

Applications

- WiMAX 802.16a
- WLAN 802.11a, 802.11b, 802.11g
- Multi-mode Radios

Options

- Kaben can incorporate a proprietary integrated Loop Filter with performance matching off-chip loop filter designs



Fractional-N Synthesizer 2 – 6 GHz

KR-SDS-60-IBM7WL-01 Data Sheet

Description

The Kaben KR-SDS-60-IBM7WL-01 Delta-Sigma ($\Delta\Sigma$) Fractional-N frequency synthesizer cell provides fine step size, low phase-noise, low spurious levels, fast switching speed, and the ability to easily integrate into your current design. This synthesizer is a key building block in designing high-performance wireless systems that require fine resolution and low power.

When integrating the $\Delta\Sigma$ Fractional-N synthesizer core into your IBM 7WL SoC, our engineers support your design for system-level integration and verification, fabrication, and maximum re-use. This proven and characterized cell helps in making your SoC design predictable and efficient across many application areas.

The Kaben KR-SDS-60-IBM7WL-01 cell has a maximum output frequency of 6 GHz while maintaining step sizes of 40 Hz using the 20-bit $\Delta\Sigma$ modulator making it ideal for 802.16a systems.

The synthesizer cell uses a high internal reference frequency of up to 40 MHz to reduce phase noise contribution. The close-in phase noise is -93 dBc/Hz at a 2 kHz offset from a 6 GHz synthesizer when using a 20

MHz reference. Spurious response of -80 dBc makes this product an ideal selection for applications where interference from adjacent or alternate channels is a significant issue.

High performance is delivered without sacrificing power consumption. The cell operates using 12.5 mA from a 2.7 V supply, with an output of 3.9 GHz and a temperature of 85 °C.

Support

Support can be provided for all phases of the life cycle of your SoC. For system design, we provide a kit that includes high-level models in Matlab/Simulink. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy. Included is a loop-filter design kit for tailoring the trade-off between VCO noise and synthesizer phase noise. All high-level models are based on measured data.

At the circuit design level, Kaben's Release Kit contains GDSII files, Verilog files, and Cadence™ design libraries containing test benches, schematics, symbols, and cell layouts. For production test, the cell has a built-in signature analysis block.

Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		2.6		3.0	V
Total Supply Current	V _{CC} = 2.7 V, Temp = 85 °C, F _{REF} = 20 MHz, F _{VCO} = 3.9 GHz		12.5		mA
RF Input Operating Frequency		2		6	GHz
Reference Oscillator Frequency	Internal Reference Oscillator			40	MHz
Charge Pump Output Current		0.0625		4	mA
Step Size			62.5		μA
Charge Pump Variation Over Temperature				+/- 5	%
RF Input Sensitivity	Peak-to-peak single ended	150		300	mV
Synthesizer contribution to close-in Phase Noise	F _{REF} = 20 MHz RF signal = 6 GHz Offset = 2 kHz Charge Pump Current = 4 mA		-93		dBc/Hz
Frequency Resolution		$\frac{F_{REF}}{2^{20}}$			Hz
Spurious	When carrier is within one Loop Bandwidth of an Integer multiple of the reference frequency			-50	dBc
	When carrier is more than 10 Loop Bandwidths away from an Integer multiple of the reference frequency		-80	-75	
Operating Temperature		-10		+125	°C

