

"An Image Reject IF Filter/Down Converter Ready for Integration into Multi-Standard Radios"

Product Description

The KR-SIF-IR-10.7-TSMC-130-01 is an IP cell that performs a filtering and down conversion functionality in a single cell.

The cell accepts a 10.7 MHz input, then bandpass filters using a 144 MHz input clock. Then, a 12 MHz output clock down samples (mixes) to a 1.3 MHz IF.

The combination of small die size of this CMOS cell coupled with no external components meets the highly competitive cost and size requirements for building successful mobile products while delivering fully integrated functionality.

Applications

- FM Radios
- Bluetooth
- GPS
- Software Defined Radios (SDR)

Features

- 10.7 MHz Center Frequency
- Output frequency 1.3 MHz
- 1 MHz Bandwidth
- Image Frequency Notch Attenuation up to 40 dB
- Programmable Gain 40 dB in 5 dB steps
- Input Intercept Point of 136 dBμV @ 96 dBμV
- Spurious Free Dynamic Range 87 dB
- Input Referred Noise 5 nV√Hz
- Linear Group Delay
- 3.0 V Operation
- Designed for TSMC 130 nm process and portable to other processes
- I2C Interface

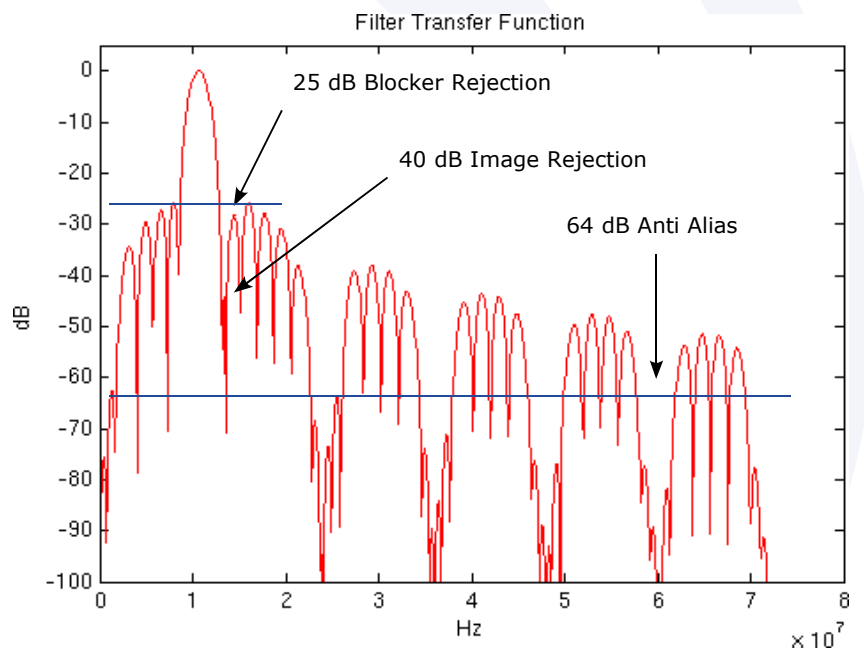
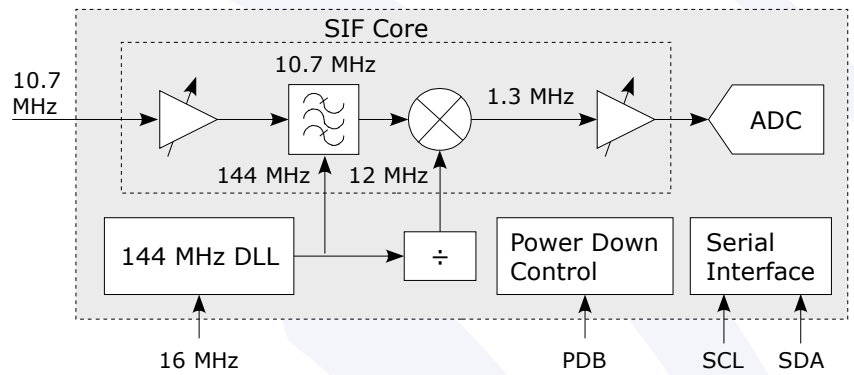


Image Reject Sampled-IF Filter/Down-Converter

KR-SIF-IR-10.7-TSMC-130-01 Product Brief

Description

Kaben's on-chip, image-reject filter/down-converter provides bandpass filtering of an input signal centered at 10.7 MHz, and down-conversion to a 1.3 MHz IF frequency, with an image-rejection attenuation up to 40 dB. The image-reject filter is based on Kaben's patented Sampling IF (SIF) technology, which enables FIR filter techniques to be realized in the analog domain.

The KR-SIF-IR-10.7-TSMC-130-01 filter consists of a SIF filter integrated with a down sampler. The filters provide image rejection and the required baseband and stop band characteristics for the incoming signal. The sampler down converts the 10.7 MHz signal to a 1.3 MHz IF frequency.

The Kaben image-reject filter/down-converter significantly improves adjacent channel rejection capability and reduces the required sample rate and resolution the associated ADC in a receiver.

Since the additional dynamic range and bandwidth required to digitize potential adjacent channel blockers (in addition to the desired signal) is no longer required, the ADC becomes smaller, the sampling clock-rate becomes lower, the overall timing precision and digitizing linearity are relaxed, and the power consumption is reduced.

Support

For system's design, we provide a kit that includes high-level models in Matlab/Simulink, or Verilog-A. System-level models offer various modes of abstraction for flexibility in simulation speed vs. accuracy.

At the circuit design level, we deliver GDS II files and a Cadence library containing schematics, symbols, and cell layouts.

Originally designed in the TSMC 130 nm process, this IP block can be ported to other technologies.

Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Input Center Frequency			10.7		MHz
Output Frequency			1.3		MHz
Image Rejection		40		45	dB
Spurious Free Dynamic Range	10 MHz Bandwidth		87		dB
Input referred IP3 (Min Gain)	Two blockers at 96 dB μ V, $ f_1-f_2 > 800$ kHz		136		dB μ V
Input Noise (Max Gain)				3	nV \sqrt Hz
Gain	5 dB steps	2		42	dB
Supply Current	Vcc = 3 V		30		mA
Supply Voltage		2.7	3.0	3.6	V
Operating Temperature		-40		85	$^{\circ}$ C

